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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,009	CHOI, JOO S.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-28 are presented for examination. This office action is in response to the application filed on 9/22/2003.

2. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

3. Applicants are requested to update the status of the related U.S. patent application referred to on page 1, accordingly (e.g., U.S. Patent Application Serial No. ##/###,### filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ##/###,###, filed on December 01, 1990, now abandoned; ...etc.). Also applicants are requested to include the status of the related U.S. applications or patents in the CROSS-REFERENCE TO RELATED APPLICATIONS section and in any other corresponding area in the specification.

Claim Objections

4. Claims 14, 12, 16, 19, 24, and 28 are objected to because of the following informalities:

As to claims 14, 12, 16, 19, 24, and 28, "substantially" should be deleted for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Raynham US Patent No. 6,418,068.

As to claim 1, Raynham discloses the invention as claimed. Raynham discloses a method, comprises receiving a command (Fig. 5 and col. 10 lines 18+)from a controller (Fig. 1 Ref. 114) to access a memory (Fig. 3); receiving, from the controller, at least one of burst length information (col. 10 line 22 and Fig. 6) and latency information (col. 10 line 23) in association with the command to access the memory; and providing data (Fig. 3 Ref. DQ0-DQ3) to or from the memory in response to the command based on at least one of the burst length information and the latency information.

As to claim 2, Raynham discloses the invention as claimed the above. Raynham further discloses wherein receiving a command comprises receiving at least one of a READ operation and WRITE operation to access the contents of the memory (col. 10 lines 18+ and Fig. 5).

As to claim 3, Raynham discloses the invention as claimed the above. Raynham further discloses wherein receiving the latency information comprises receiving at least one of column address strobe latency information and write latency information (Fig. 6).

As to claim 4, Raynham discloses the invention as claimed the above. Raynham further discloses wherein receiving at least one of the burst length information and the latency information in association with the command to access the memory comprises receiving at least one of the burst length information and the latency information substantially contemporaneously with the command to access the memory (Fig. 6).

As to claim 5, Raynham discloses the invention as claimed the above. Raynham further discloses wherein receiving the burst length information comprises receiving a burst length information based on an amount of data to be retrieved from the memory (Fig. 6).

As to claim 6, Raynham discloses the invention as claimed the above. Raynham further discloses wherein receiving the burst length information comprises receiving a burst length of a first preselected value in response to the controller receiving a request from a peripheral client and a burst length of a second preselected value in response to the controller receiving a request from a main client, wherein the first preselected value is less than the second preselected value (Fig. 6, Burst length could be combinations of 3 binary bits).

As to claim 7, Raynham discloses the invention as claimed the above. Raynham further discloses wherein receiving at least one of the burst length information and latency information comprises receiving the information over a redundant address line to the memory (Fig. 1 Ref. 142 & Refs. 146's and Fig. 6, A11. Also In Fig. 3 address lines A0-A11 are provided to mode registers, row address mux and column address counter at different time frame for the purpose of saving input pin count).

As to claim 8, Raynham discloses the invention as claimed the above. Raynham further discloses wherein receiving the information over the redundant address line comprises receiving the information over a redundant row address line (Fig. 6, A11).

As to claim 9, Raynham discloses the invention as claimed the above. Raynham further discloses wherein receiving the information over the redundant address line comprises receiving the information over a redundant column address line (Fig. 6, A11)

As to claim 10, Raynham discloses the invention as claimed. Raynham discloses an apparatus, comprises a controller (Fig. 1 Ref. 114) adapted to: provide a command (Fig. 5) to access a memory array (Fig. 3); provide at least one of burst length information (Fig. 6) and latency information (Fig. 6) in association with the command to access the memory array; and receive (Fig. 3 DQ0-DQ3) data from the

memory array in response to the command based on at least one of the burst length information and the latency information.

As to claim 11, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the controller is adapted to issue a READ operation access the contents of the memory (Fig. 5).

As to claim 12, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the controller is adapted to provide at least one of the burst length information and the latency information substantially contemporaneously with the command to access the memory (col. 10 lines 18+, Fig. 5 and Fig.6).

As to claim 13, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the controller is adapted to provide a burst length of a first preselected value in response to receiving a request from a peripheral client and a burst length of a second preselected value in response to receiving a request from a main client, wherein the first preselected value is less than the second preselected value (Fig. 6, Burst length could be combinations of 3 binary bits).

As to claim 14, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the controller is adapted to provide at least one of

the burst length information and latency information over a redundant address line to the memory (Fig. 1 Ref. 142 & Refs. 146's and Fig. 6, A11).

As to claim 15, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the controller is adapted to provide at least one of the burst length information and latency information over at least one of a redundant column address line and a redundant row address line (Fig. 6, A11).

As to claim 16, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the controller is adapted to issue a WRITE command and adapted to provide write latency information substantially contemporaneously with the WRITE command (Fig. 5 and col. 10 line 25 programmed reads on this limitation).

As to claim 17, Raynham discloses the invention as claimed. Raynham discloses a system, comprises a memory array (Fig. 3), and a controller (Fig. 1 ref. 114) communicatively coupled to the memory array, the controller adapted to: provide a command (Fig. 5) to access the memory array; and provide at least one of burst length information and latency information (Fig. 6) in association with the command to access the memory array; and wherein the memory array is adapted to provide or receive data (Fig. 3 Ref. DQ0-DQ3) in response to the command based on at least one of the burst length information and the latency information.

As to claim 18, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the controller is adapted to issue at least one of a READ operation and WRITE operation access the contents of the memory (Fig. 5).

As to claim 19, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the controller is adapted to provide at least one of the burst length information and the latency information substantially contemporaneously with the command to access the memory (Fig. 6 and col. 10 line 25 programmed reads on this limitation).

As to claim 20, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the controller is adapted to provide a burst length of a first preselected value in response to receiving a request from a peripheral client and a burst length of a second preselected value in response to receiving a request from a main client, wherein the first preselected value is less than the second preselected value (Fig. 6, Burst length could be combinations of 3 binary bits).

As to claim 21, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the controller is adapted to provide at least one of the burst length information and latency information over a redundant address line to the memory (Fig. 1 Ref. 142 & Refs. 146's and Fig. 6, A11).

As to claim 22, Raynham discloses the invention as claimed. Raynham discloses an apparatus, comprises means for providing a command (Fig. 5) from a controller (Fig. 1 Ref. 114) to access a memory (Fig. 3); means for providing, from the controller, at least one of burst length information and latency information (Fig. 6) in association with the command to access the memory; and means for providing data (Fig. 3 Ref DQ0-DQ3) to or from the memory in response to the command based on at least one of the burst length information and the latency information.

As to claim 23, Raynham discloses the invention as claimed. Raynham discloses an apparatus, comprises a memory (Fig. 3) adapted to: receive a command (Fig. 5) from a memory controller (Fig. 1 Ref. 114) to access contents of the memory; receive, from the memory controller, at least one of burst length information and latency information (Fig. 6) in association with the command to access the contents; and provide data (Fig. 3 Ref DQ0-DQ3) from the memory in response to the command based on at least one of the burst length information and the latency information.

As to claim 24, Raynham discloses the invention as claimed the above. Raynham further discloses wherein memory is adapted to receive at least one of the burst length information and the latency information substantially contemporaneously with the command to access the memory (Fig. 5).

As to claim 25, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the memory is adapted to receive a burst length of a first preselected value in response to the controller receiving a request from a peripheral client and a burst length of a second preselected value in response to the controller receiving a request from a main client, wherein the first preselected value is less than the second preselected value (Fig. 6, Burst length could be combinations of 3 binary bits).

As to claim 26, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the memory is adapted to receive at least one of the burst length information and latency information over a redundant address line (Fig. 1 Ref. 142 & Refs. 146's and Fig. 6, A11).

As to claim 27, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the memory is adapted to receive at least one of the burst length information and latency information over at least one of a redundant column address line and a redundant row address line (Fig. 1 Ref. 142 & Refs. 146's and Fig. 6, A11).

As to claim 28, Raynham discloses the invention as claimed the above. Raynham further discloses wherein the memory is adapted to receive a WRITE command and adapted to receive write latency information substantially

contemporaneously with the WRITE command (Fig. 5 and col. 10 line 25 programmed reads on this limitation).

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(571)-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

H Kim
Primary Patent Examiner
November 22, 2005